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PTO/SB/08A (08-00)

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Sheet 1 of 2

Complete if Known	
Application Number	10/743894
Filing Date	12/17/2003
First Named Inventor	Madurawe, Raminda U.
Group Art Unit	2819
Examiner Name	D. de
Attorney Docket Number	

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

**Examiner
Signature**

Don E

**Date
Considered**

8/5/05

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¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet

2

of

2

Complete if Known

Application Number 101793894

Filing Date 12/17/2003

First Named Inventor: Madurawwa, Raminda H.

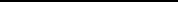
Group Art | Unit

Group A1 Unit

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
he		SEALS & WHAPSHOTT, "Programmable Logic - PLDs and FPGAs", 1997, pp 102-117, McGraw-Hill, USA.	<input type="checkbox"/>
p7		ASHOK K. SHARMA, "Programmable Logic Handbook - PLDs, CPLDs, & FPGAs", 1998, pp 99-171, McGraw-Hill, USA.	<input type="checkbox"/>
lw		E. AHMED, J. ROSE, "The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density", FPGA 2000, Monterey, CA, 2000.	<input type="checkbox"/>
			<input type="checkbox"/>

Examiner Signature			Date Considered	8/5/95
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